SPECIFICATION FOR SUPER XE GAME MACHINE.

JUNE 21 '88
RICOH

OBJECTS

64 OBJECTS / FRAME

16 OBJECTS / LINE

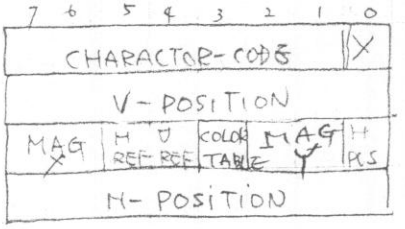
16 COLORS / OBJECTS

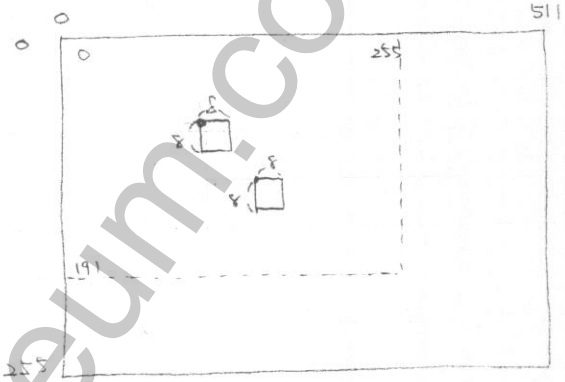
32 COLORS / FRAME *

2^{12} COLORS / POSSIBILTY

X1, X2, X4 (MAX X4)

H REF. V REF
8 X 8 PIXCEL / OBTECT (X1)





BACK GROUND

1 CELL MAP

40 CHARACTOR X 24 CHARACTOR / FRAME

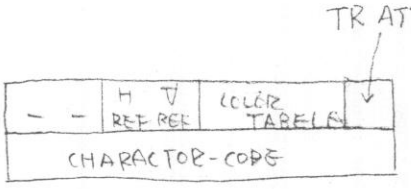
4 COLORS / CHARACTOR

8 X 8 pixel / CHARACTOR

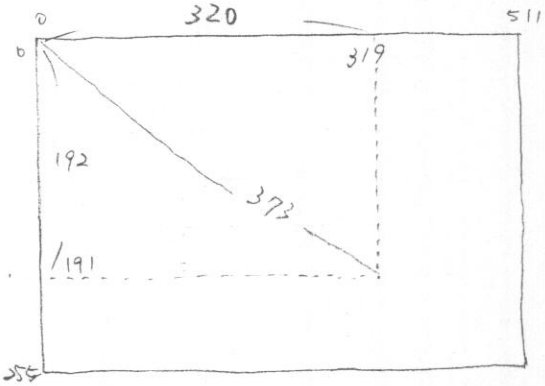
32 COLORS / FRAME *

2^{12} COLORS / POSSIBILTY

H. REF. V REF



FRAME MEMORY
64 CHARACTOR X 32 CHARACTOR
2 Byte / CHARACTOR
4k Byte / FRAME



PATTERN MEMORY
2bit / pixel
16Byte / CHARACTOR
256 CHARACTOR / FRAME *

* DYNAMICALY CHENGEABLE

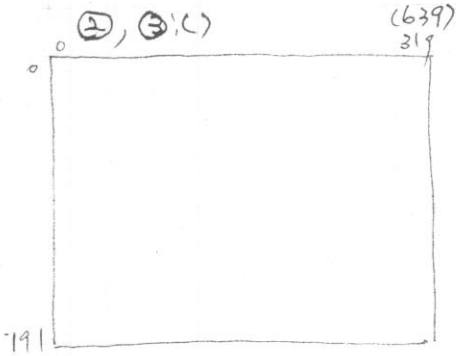
2. Bit MAP

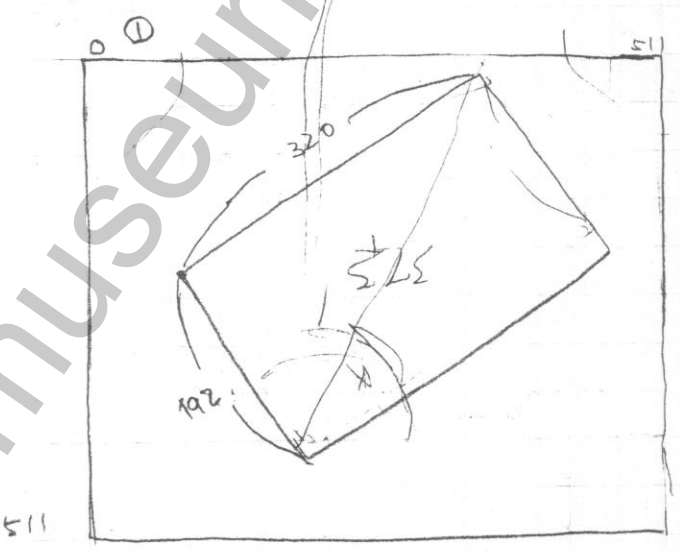
Memory size
512 dot × 512 dot × 4bit

① 320 × 192 pixel / FRAME
~~# #~~ COLORS / pixel
16
with ROTATE CPU RUN TIME ≒ 0%

② 320 × 192 pixel / FRAME
~~#~~ COLORS / pixel
16
320 dot —
without ROTATE CPU RUN TIME ≒ 50%

③ 640 × 192 pixel / FRAME
4 COLORS / pixel
640 dot —
without ROTATE CPU RUN TIME ≒ 50%

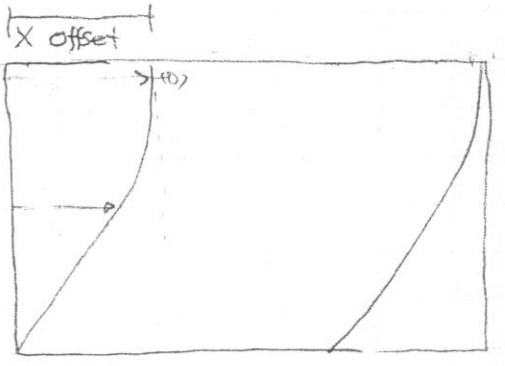


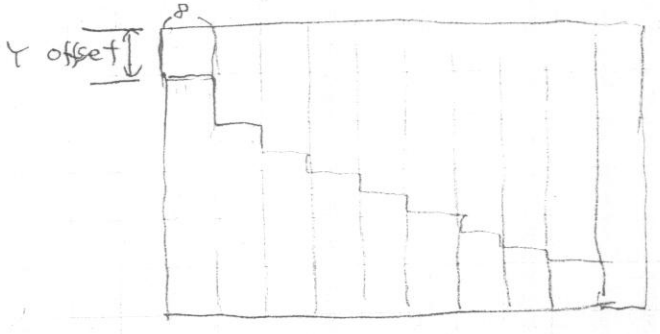


3. OTHERS (cell map)

LINE FLOWING

VERTICAL FLOWING





CPU

65C816

A. 8MHz INSIDE RAM
B. 4MHz OUTSIDE MEMORY
C 1.71 MHz 65XE MODE

A and B be chenged by cpu Address.

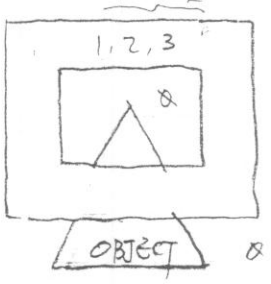
512bit SRAM

SOUND. (See pages 5 ~ 7.)

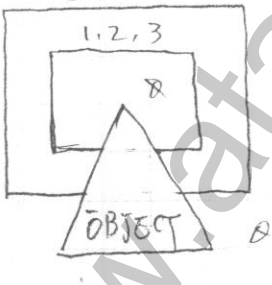
(contd Page 2')

4. Cell map

TR. ATTRIBUTE. SET 1 (IN CHARCTOR GEN) COLOR CODE



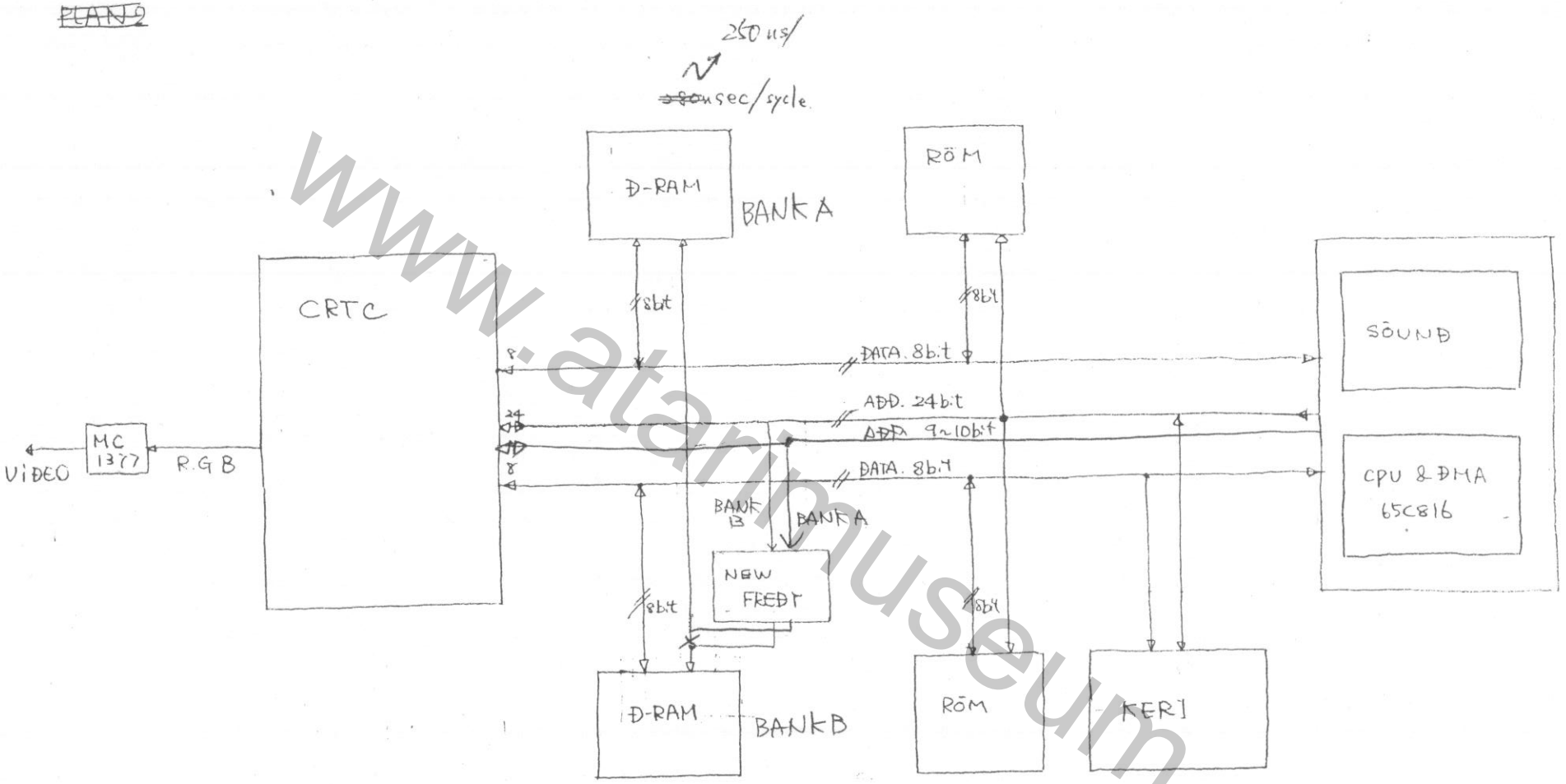
TR. ATTRIBUTE SET 0



5. Border color control Register (12bit)

Besides Color L.U.T

~~PLAN 2~~



SYSTEMS CONFIGURATION

A. 65XE Mode of Operation

B. Extended Mode of Operation

Video features

~~1) Display List Architecture.~~

~~2) Lumenance & Chromanence outputs.~~ → external

3) Analog RGB output ~~& composite video output.~~

4) 640 dot mode ~~line buffer.~~ bitmap

5) Object size multiplier x2, x4. (MAX x4)

6) Run microprocessor at 2x clock of 65xE mode. 4x

~~7) 3-D mode.~~

8) Object reflection.

9) Line Buffers.
   a. 320x~~8 with~~ objects.
      x5 bit for

Audio Features

1) Sound output in stereo.

2) 8 channel P.C.M. sound. (depends on Cost)

3) Programmable sampling rate.

I/O Support

*Not required as the "Keri" Chip will be used.

General description:

Stereo digitized sound (256 level) is stored interleaved (high byte = left channel, low byte = right channel) in contiguous memory, this data is supplied directly to two Digital-to-Analog Converters at a fixed rate (the sampling frequency). The output of the DACs are low pass filtered and provided to the speakers.

Sampling Frequency:

In order to allow for both hi quality sound and simple beeps without requiring huge quantities of data, four sampling rates will be provided:

~~40053 Hz~~
~~20027 Hz~~ → 19,8 KHz
10013 Hz
5006 Hz

These are independent of video mode and destination country (NTSC/PAL). The 3dB cutoff for the low pass filter will always be at 1/2 the sampling frequency.

Address Control:

There are two sets of registers which control the supply of data to the DAC. First is a base register, similar to the video base register, which points to the start of data. Second is a length which specifies the number of words to fetch before repeating the pattern. The base register can be loaded at any time but will not take effect until the length reaches zero or DMA is initially started. Thus it can be loaded during playback to chain pieces of sound together. The same thing applies to the length. The address and length are both 23-bit registers.

In addition to the base register, there is a read-only register which contains the current address to be fetched.

DMA Control:

A single bit is provided to enable DMA. When set DMA will start using the current base address and length. When cleared DMA will stop AT THE NEXT zero count. DMA will be disabled at reset.

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Volume:

An 8 bit master volume register will be provided to scale the outputs of both DACs. Zero will be off and 255 will be full on. This register will be zeroed at reset.

QUESTIONS:

1. Does software require any interrupts to effectively use this scheme?
2. Is stereo necessary? Desirable? Yes Yes
3. Should a mode be provided to allow the same data to be provided to both channels simultaneously? (Mono mode) Yes
4. Can the length in a "mono mode" still be word oriented? That is, can you live with the restriction that there must be an even number of samples in mono mode? 1
5. Is a mode which would allow one channel to modulate the amplitude of the other desirable? 2

Answer next meeting

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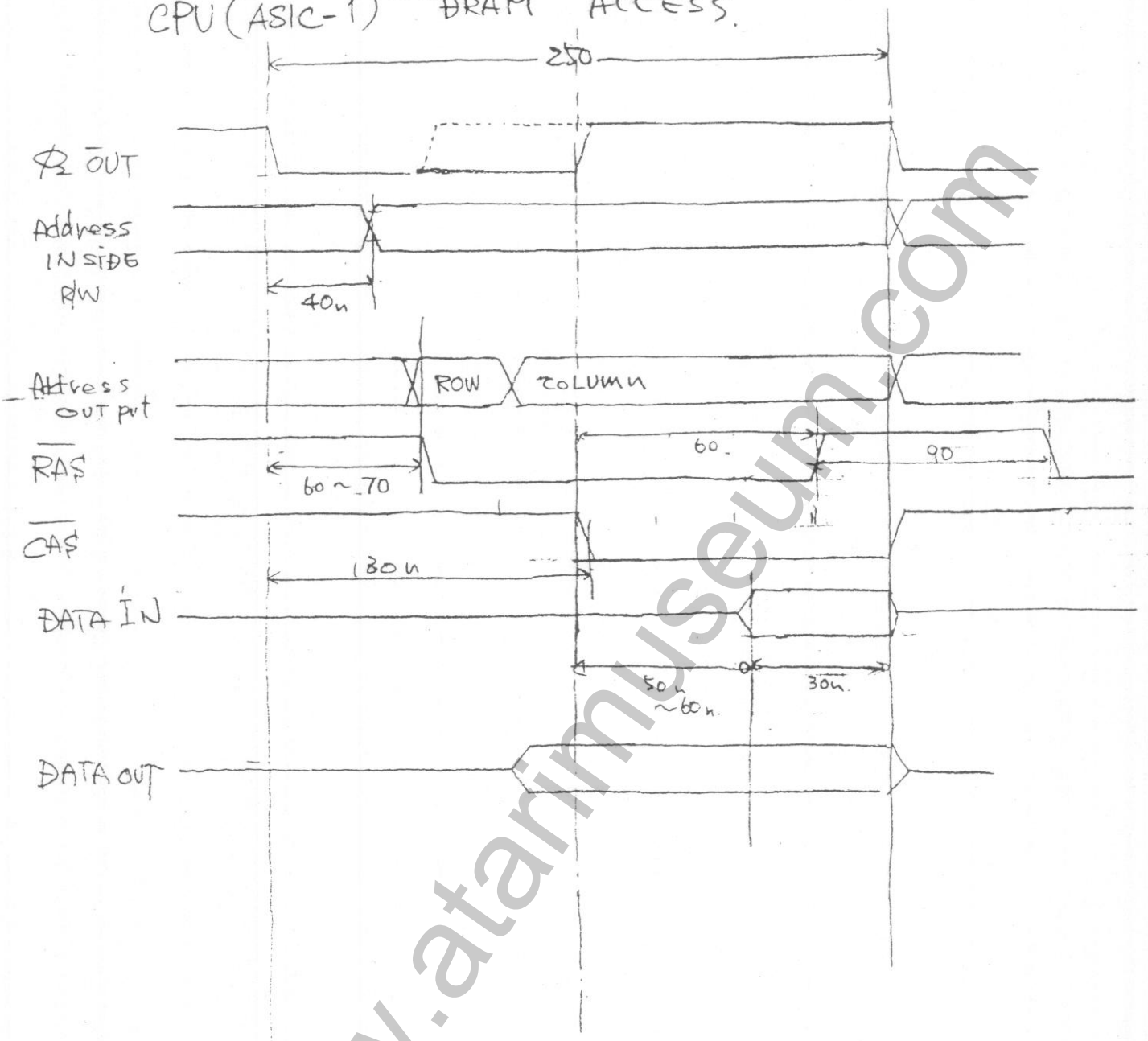
CPU (ASIC-1) DRAM ACCESS.



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